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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,783	03/12/2004	Jin-Kyoung Jung	SAM-0529	8323

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02/09/2007

EXAMINER

ALMO, KHAREEM E

ART UNIT

PAPER NUMBER

2816

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/799,783

Applicant(s)

JUNG ET AL.

Examiner

Khareem E. Almo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 7-12, 14-16, 23, 25 and 27-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 7-12, 14-16, 23, 25 and 27-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 and 18 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed on 11/9/2006 has been received and entered in the case.
2. The indicated allowability of claims 1-3, 7-9 and 30-38 are withdrawn in view of the newly discovered reference(s) to Rhee et al.(US 6774712). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Rhee et al. (US 6774712).

With respect to claim 1, Figure 4 of Rhee discloses a semiconductor device, comprising: a control signal generating circuit (outputting PDPDEB) for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal

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voltage generating circuit (61) coupled to the control signal (PDPDEB), the internal voltage generating circuit comprising: a comparing circuit (51) for comparing a reference voltage (output from 41) to an internal voltage (IVC) to generate a driving signal (output at 60) when the control signal is inactivated, wherein the comparing circuit comprises: a comparator (52) connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and a switching circuit (58) connected between an external power voltage (+) applied to the comparator when the control signal is activated; a driving signal control circuit (60) for inactivating the driving signal when the control signal is activated; and an internal voltage driving circuit (53) for receiving the external power voltage (+) and generating the internal voltage in response to the driving signal.

With respect to claim 3, figure 4 discloses the device of claim 1, wherein the internal voltage driving circuit (54) includes a PMOS transistor which has a source to which the external power voltage (+) is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage (IVC) wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to a external power voltage level when the driving signal is inactivated.

With respect to claim 7-9, these claims are deemed to be intended use.

With respect to claims 30-32, these claims are deemed to be intended use.

(Note: any value or number of bits input would correspond to the number of bits

processed by the semiconductor because the input and the value of the bits have a causal effect on the semiconductor.)

With respect to claims 34-35 and 37 are rejected for similar reasons as above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. (US 6774712) in view of Bae et al. (US 6373754).

With respect to claim 2, figure 4 teaches the device of claim 1, wherein the driving signal control circuit includes a transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied and a source connected to a voltage. Bae et al. teaches the use of an NMOS or a PMOS interchangeable to control the driving signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a NMOS instead of a PMOS as the driving signal control circuit, for the purpose changing the activation signal.

7. Claims 33, 36 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee et al. in view of Park et al. (US 5349559)

With respect to claims 33, 36 and 38, figure 4 of Rhee et al. discloses the circuit above, but fails to disclose wherein the circuit comprises a second switching device. Figure 4 of Park et al teaches the use of a dual transistor CMOS switch to drive a internal control signal. It would have been obvious at the time the invention was made to a person having ordinary skill in the art, to use any switch to the driving of the internal voltage driving signal circuit, for the purpose of stability in the switching process.

8. Claims 10-12, 14-17, 23, 25 and 27-29 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (20020053943) in view of Sher (US 6633196).

With respect to claim 10, figure 1 and 5a of Yamasaki discloses a semiconductor device comprising; a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE), the internal voltage generating circuit comprising a comparing circuit (CMP) for comparing a reference voltage (Vref) to an internal voltage (IntVcc) to generate a comparing signal; a switching circuit (DR)

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coupled to an output of the comparing circuit for transmitting the comparing signal as a driving signal when the control signal (TE) is inactivated and a driving signal control circuit (2) for inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal but fails to disclose wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to claim 11, the above circuit produces the circuit of claim 10 wherein the driving signal control circuit includes an NMOS transistor (2f) which has a drain connected to the driving signal generating terminal (via 2ba) for generating the driving signal, a gate to which the control signal (TE) is applied, and a source connected to a ground voltage.

With respect to claim 12, the above circuit produces the circuit of claim 10 wherein the internal voltage driving circuit includes a PMOS transistor (DR) which has a source to which the external power voltage is applied (EX) a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage (IntVcc) wherein the PMOS transistor turns the internal voltage to a

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reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage when the driving signal is inactivated.

With respect to claim 14, the above circuit produces the circuit of claim 10 but fails to produce the circuit wherein the input signal is generated using a fuse. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal for the purpose of making the input signal irreversible.

With respect to claim 15, the recitation of the input signal being generated by an external pad is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 16, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

With respect to claim 23, figure 1 and 5a of Yamasaki discloses a control signal generating circuit (5a) for generating a control signal (TE) responsive to an input signal (/RAS, /CAS, /WE or Add) related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor

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device is less than the predetermined number of bits; and an internal voltage generating circuit (Figure 1) coupled to the control signal generating circuit for receiving the control signal (TE) and comparing a reference voltage (V_{ref}) to an internal voltage ($IntV_{cc}$) to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, wherein the internal voltage generating circuit comprises at least one of a first switching circuit (2e) that cuts off an external power voltage applied to the internal voltage generating circuit when the control signal (TE) is activated, a second switching circuit (2f) that cuts off a ground voltage supplied to the internal voltage generating circuit when the control signal (TE) is activated and a third switching circuit (2c) but fails to disclose the third switching circuit including a CMOS transmission gate which transmits the driving signal when the control signal is inactivated. Figures 3a and 3b of Sher teaches the use of CMOS transmission gates for NMOS transistor switching elements. It would have been obvious at the time the invention was made to one of ordinary skill in the art to substitute the NMOS switching elements of Yamasaki with CMOS transmission gates for the purpose of improving switching speed.

With respect to 25, the circuit above produces the circuit of claim 23, wherein the internal voltage generating circuit includes a comparing circuit (CMP) for comparing the reference voltage to the internal voltage ($IntV_{cc}$) to generate a comparing signal; a switching circuit (DR) for transmitting the comparing signal as a driving signal when the control signal is control signal is inactivated; a driving signal control circuit (2) for

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inactivating the driving signal when the control signal is activated and an internal voltage driving circuit (RFG, Figure 20) for receiving an external power voltage (EX) and generating the internal voltage in response to the driving signal.

With respect to claim 27, the above circuit produces the circuit of claim 23 but fails to produce the circuit wherein the input signal is generated using a fuse. It is well known in the art to use a laser burned fuse to generate an irreversible signal that can be controlled externally. It would have been obvious at the time the invention was made to one of ordinary skill in the art to use a fuse to generate an input signal for the purpose of making the input signal irreversible.

With respect to claim 28, the recitation of the input signal being generated by an external pad is deemed to be inherent because in a semiconductor device an external pad is inherently used to connect to circuits.

With respect to claim 29, the circuit above produces the circuit of claim 23, wherein the control signal generating circuit (5a) activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command. (See paragraphs [0093] and [0094]).

Response to Arguments

9. Applicant's arguments filed 11/9/2007 have been fully considered but they are not persuasive.

With respect to applicant's arguments Yamassaki et al. and Sher, fail to teach or suggest a control signal generating circuit for generating a control signal responsive to

an input signal related to a number of bits being processed by a semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed the Examiner disagrees.

With respect to applicant's argument there is no teaching or suggestion in Yamasaki, et al. of the row address strobe signal /RAS column address strobe signal /CAS, write enable signal /WE, or specific address signal bit AD being an input signal related to a number of bits processed by a semiconductor device, the Examiner disagrees. The Examiner further notes that these signals are shown specifically as input signals and that they inherently are related to the number of bits processed by the semiconductor because they are bits and function so that the processor reacts in response to the number of bits each signal contains. {See 0092-0094} Since these signals are bits, and depending on the way the bits are set activate the control signal, the device is related to the number of bits being processed by the semiconductor as claimed.

With respect to applicant's argument there is no teaching or suggestion in Yamasaki et al. of the test mode designating signal TE being activated when an input signal indicates that a number of data bits being processed by a semiconductor device is more than a predetermined number of bits, and the test mode designating signal TE being inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits,

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the Examiner disagrees. Since the signal is activated by a predetermined number of bits and in the claims the specific number is not specified the number of bits can be any number. Therefore this limitation is satisfied.

With respect to applicant's argument there is no teaching or suggestion of the control voltage V_{select} being activated when an input signal indicates that a number of data bits being processed by a semiconductor device is more than a predetermined number of bits, and the control voltage V_{select} being inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less than the predetermined number of bits, as claimed, the Examiner disagrees. Since the signal is activated by a predetermined number of bits and in the claims the specific number is not specified, the number of bits can be any number. Therefore this limitation is satisfied since the control voltage is activated based on a predetermined number of bits.

With respect to applicant's argument Yamassaki et al and Sher fail to teach or suggest a switching circuit coupled to an output of a comparing circuit for transmitting a comparing signal as a driving signal when the control signal is inactivated, the Examiner disagrees. The switching circuit (DR) is coupled to the output of the comparing circuit (CMP). Furthermore the when TE is inactivated the IVL signal is driving the element connected to it.

With respect to applicant's arguments Neither Yamasaki et al. no Sher teaches a control signal as claimed, the Examiner disagrees as above.

With respect to applicant's argument there is no teaching or suggestion in Yamasaki et al. of drive transistor DR transmitting a comparing signal as a driving signal when the control signal is inactivated, the Examiner disagrees. It is apparent that the switching circuit (DR) is transmitting a comparing signal (IVL) as a driving signal during the time when TE is inactive.

With respect to applicant's arguments Yamasaki et al. fails to teach a switching circuit coupled to an output of a comparing circuit, the Examiner disagrees. The switching circuit is clearly PMOS DR.

With respect to applicant's argument Sher fails to teach a switching circuit coupled to an output of a comparing circuit, the Examiner agrees. However, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore again, this argument is not persuasive.

With respect to applicants argument Yamasaki et al. and Sher fail to teach or suggest a control signal generating circuit for generating a control signal responsive to an input signal related to a number of bits being processed by the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being processed by the semiconductor device is more than a predetermined number of bits, and the control signal is inactivated when the input signal indicates that the number of bits being processed by the semiconductor device is less

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than the predetermined number of bits, as claimed in independent claim 23, the Examiner disagrees for similar reasons as stated above.

With respect to applicant's arguments the prior art fails to teach or suggest an internal voltage generating circuit coupled to a control signal generating circuit for receiving a control signal and comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, and to make the internal voltage have an external power voltage level when the control signal is activated, the Examiner disagrees, for similar reasons as stated above.


10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


KEA
2/1/2007


Quan Tra
Primary Examiner